CLAIMS

What is claimed is:

1   1.   A method for execution by a microprocessor in response to receiving a single

2   instruction, the method comprising:

3   receiving a first plurality of numbers and a second plurality of numbers, each

4   of the first plurality of numbers pointing to one of a plurality of

5   entries, each of the plurality of entries being in one of a plurality of

6   look-up tables; and

7   replacing simultaneously the plurality of entries in the plurality of look-up

8   tables with the second plurality of numbers;

9   wherein the above operations are performed in response to the

10   microprocessor receiving the single instruction.

1   2.   A method as in claim 1 wherein the first plurality of numbers are received

2   from a first entry in a register file; and the second plurality of numbers are

3   received from a second entry in the register file; and wherein the

4   microprocessor is a media processor integrated with a memory controller on

5   a single integrate circuit.

1   3.   A method as in claim 2 wherein the single instruction specifies indices of the

2   first and second entries in the register file.

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1   4.   A method for execution by a microprocessor in response to receiving a single

2   instruction, the method comprising:

3   replacing at least one entry in at least one of a plurality of look-up units in a

4   microprocessor unit with at least one number using a Direct Memory

5   Access (DMA) controller;

6   wherein the above operations are performed in response to the

7   microprocessor receiving the single instruction.

1   5.   A method for execution by a microprocessor in response to receiving a single

2   instruction, the method comprising:

3   replacing at least one entry for each of a plurality of look-up units in a

4   microprocessor with a plurality of numbers using a Direct Memory

5   Access (DMA) controller;

6   wherein the above operations are performed in response to the

7   microprocessor receiving the single instruction.

1   6.   A method as in claim 5 wherein a single index encoded in the instruction

2   specifies a location of the at least one entry in the plurality of look-up units.

1   7.   A method as in claim 5 wherein a single index encoded in the instruction

2   specifies a total number of the at least one entry for each of a plurality of

3   look-up units.

1   8.   A method as in claim 5 wherein a source address of the plurality of numbers

2   is specified in an entry of a register file.

1   9.   A method as in claim 8 wherein the single instruction specifies an index of

2   the entry in the register file.

1   10.   A method as in claim 5 wherein an identity number encoded in the single

2   instruction specifies the DMA controller.

1   11.   A method for execution by a microprocessor in response to receiving a single

2   instruction, the method comprising:

3   receiving a plurality of numbers;

4   partitioning look-up memory into a plurality of look-up tables;

5   looking up simultaneously a plurality of elements from the plurality of look-

6   up tables, each of the plurality of elements being in one of the

7   plurality of look-up tables and being pointed to by one of the plurality

8   of numbers;

9   wherein the above operations are performed in response to the

10   microprocessor receiving the single instruction.

1   12.   A method as in claim 11 wherein the receiving a plurality of numbers

2   comprises:

3   partitioning a string of bits into a plurality of segments to generate the

4   plurality of numbers.

1 13. A method as in claim 12 wherein the single instruction specifies format

2   information in which the plurality of numbers are stored in the string of bits.

1 14. A method as in claim 11 wherein the look-up memory comprises a plurality

2   of look-up units, and wherein said partitioning look-up memory comprises:

3   configuring the plurality of look-up units into the plurality of look-up tables.

1 15. A method as in claim 11 wherein the string of bits is received from an entry

2   of a register file.

1 16. A method as in claim 15 wherein the single instruction specifies an index of

2   the entry.

1 17. A method as in claim 11 further comprising:

2   storing the plurality of elements in an entry of a register file.

1 18. A method as in claim 17 wherein the single instruction specifies an index of

2   the entry.

1   19.   A method as in claim 17 wherein the single instruction specifies format

2   information in which the plurality of elements are stored in the entry.

1   20.   A method as in claim 14 wherein each of the plurality of look-up units

2   comprises 256 8-bit entries.

1   21.   A method as in claim 11 wherein the single instruction specifies a total

2   number of entries contained in each of the plurality of look-up tables.

1   22.   A method as in claim 21 wherein the total number of entries is one of:

2   a) 256;

3   b) 512; and

4   c) 1024.

1   23.   A method as in claim 11 wherein the single instruction specifies a total

2   number of bits used by each entry contained in the plurality of look-up tables.

1   24.   A method as in claim 21 wherein the total number of bits is one of:

2   a) 8;

3   b) 16; and

4   c) 24.

1 25. A machine readable media containing an executable computer program

2 instruction which when executed by a digital processing system causes said

3 system to perform a method comprising:

4 receiving a first plurality of numbers and a second plurality of numbers, each

5 of the first plurality of numbers pointing to one of a plurality of

6 entries, each of the plurality of entries being in one of a plurality of

7 look-up tables; and

8 replacing simultaneously the plurality of entries in the plurality of look-up

9 tables with the second plurality of numbers;

10 wherein the above operations are performed in response to the

11 microprocessor receiving the single instruction.

1 26. A media as in claim 25 wherein the first plurality of numbers are received

2 from a first entry in a register file; and the second plurality of numbers are

3 received from a second entry in the register file.

1 27. A media as in claim 26 wherein the single instruction specifies indices of the

2 first and second entries in the register file.

1 28. A machine readable media containing an executable computer program

2 instruction which when executed by a digital processing system causes said

3 system to perform a method comprising:

4   replacing at least one entry in at least one of a plurality of look-up units in a

5   microprocessor unit with at least one number using a Direct Memory

6   Access (DMA) controller;

7   wherein the above operations are performed in response to the

8   microprocessor receiving the single instruction.

1 29. A machine readable media containing an executable computer program

2   instruction which when executed by a digital processing system causes said

3   system to perform a method comprising:

4   replacing at least one entry for each of a plurality of look-up units in a

5   microprocessor with a plurality of numbers using a Direct Memory

6   Access (DMA) controller;

7   wherein the above operations are performed in response to the

8   microprocessor receiving the single instruction.

1 30. A media as in claim 29 wherein a single index encoded in the instruction

2   specifies a location of the at least one entry in the plurality of look-up units.

1 31. A media as in claim 29 wherein a single index encoded in the instruction

2   specifies a total number of the at least one entry for each of a plurality of

3   look-up units.

1　32.　A media as in claim 29 wherein a source address of the plurality of numbers

2　　　is specified in an entry of a register file.

1　33.　A media as in claim 32 wherein the single instruction specifies an index of

2　　　the entry in the register file.

1　34.　A media as in claim 29 wherein an identity number encoded in the single

2　　　instruction specifies the DMA controller.

1　35.　A machine readable media containing an executable computer program

2　　　instruction which when executed by a digital processing system causes said

3　　　system to perform a method comprising:

4　　　receiving a plurality of numbers;

5　　　partitioning look-up memory into a plurality of look-up tables;

6　　　looking up simultaneously a plurality of elements from the plurality of look-

7　　　　　up tables, each of the plurality of elements being in one of the

8　　　　　plurality of look-up tables and being pointed to by one of the plurality

9　　　　　of numbers;

10　　　wherein the above operations are performed in response to the

11　　　　　microprocessor receiving the single instruction.

1   36.   A media as in claim 35 wherein said receiving a plurality of numbers

2   comprises:

3   partitioning a string of bits into a plurality of segments to generate the

4   plurality of numbers.

1   37.   A media as in claim 36 wherein the single instruction specifies format

2   information in which the plurality of numbers are stored in the string of bits.

1   38.   A media as in claim 35 wherein the look-up memory comprises a plurality of

2   look-up units, and wherein said partitioning look-up memory comprises:

3   configuring the plurality of look-up units into the plurality of look-up tables.

1   39.   A media as in claim 35 wherein the string of bits is received from an entry of

2   a register file.

1   40.   A media as in claim 39 wherein the single instruction specifies an index of

2   the entry.

1   41.   A media as in claim 35 wherein the method further comprises:

2   storing the plurality of elements in an entry of a register file.

1 42. A media as in claim 41 wherein the single instruction specifies an index of

2   the entry.

1 43. A media as in claim 41 wherein the single instruction specifies format

2   information in which the plurality of elements are stored in the entry.

1 44. A media as in claim 38 wherein each of the plurality of look-up units

2   comprises 256 8-bit entries.

1 45. A media as in claim 35 wherein the single instruction specifies a total

2   number of entries contained in each of the plurality of look-up tables.

1 46. A media as in claim 45 wherein the total number of entries is one of:

2   a) 256;

3   b) 512; and

4   c) 1024.

1 47. A media as in claim 35 wherein the single instruction specifies a total

2   number of bits used by each entry contained in the plurality of look-up tables.

1 48. A media as in claim 47 wherein the total number of bits is one of:

2   a) 8;

3   b) 16; and

4   c) 24.